

Time-to-Digital-Converter (TDC) with USB 2.0 interface:

The USB2.0-TDC combines the excellent performance of the TDC-GPX with a high speed USB interface. Optional, a programmable logic unit (PLU) enables comfortable data preconditioning and a variable data stream handling via USB 2.0.

TDC basic device features:

- LVTTTL or PECL inputs, common start input usable as reset of the internal clock
- internal clock quartz-accurate, resolution adjust PLL, i.e. insensitive to temperature / voltage variations, adjustable via software (no calibration necessary)
- 8 stop channels at resolution of 81 ps, measurement range 0 ns – 10.6 μs in start-stop operation (double TDC option: 16 stop channels, 2 start channels)
- 2 stop channels at resolution of 27 ps, measurement range 0 ns – 3.5 μs in start-stop operation (double TDC option: 4 channels, 2 start channels)
- M-Mode at 10 ps standard deviation, with 2 stop channels (when start – stop time interval exceeds typ. 120 ns)
- min. time between start and stop 0 ns, pulse pair resolution 5.5 ns, min. 32 hits/ch
- multi-hit capability extendable by FPGA option (e.g. hit tagging, see options)
- no minimum time limit for hits at different channels
- measurement rate up to 5 million results per second via USB 2.0 (up to 40 mrps optional, using FPGA features, see options)

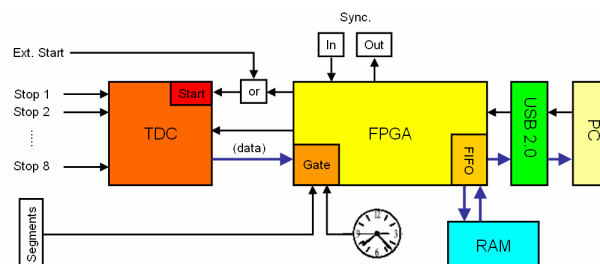
Options (as single or combined options available):

1. Dual TDC-Option: 2 TDCs in one device at one readout unit providing 16 channels (81 ps each) or 4 channels (10 ps, 27 ps each)

2. PLU-Option: FPGA pre-conditioning feature, enables extended functionality, e.g. (in some extend user specific features are possible):

- 40 MHz data acquisition rate using the FPGA pre-conditioning
- additional I/O lines for streaming of logical states or with counters
- quartz stabilized, free programmable, global time gate (100 ns – 24 h)
- free programmable primary input gate of the PLU (10 ns – 50 μs)
- free programmable channel pairing, pair arithmetic, result range limiting

Fig. 1: Principle for including a FPGA based extended functionality (PLU - Option)



Technical data of basic operational modes:

4 different operation modes, 81 ps up to 10 ps resolution

I-Mode

- * 8 channels with 81 ps BIN (INL 1 LSB)
- * 5.5 ns pulse-pair resolution with 32-fold multi-hit capability = 200 MHz peak rate
- * Trigger to rising or falling edge
- * Endless measurement range by internal retrigger of START

R-Mode

- * 2 channels with 27 ps BIN (INL 1 LSB)
- * Measurement range 0 ns up to > 10 μ s
- * 5.5 ns pulse-pair resolution with 32-fold multi-hit capability 200 MHz peak rate
- * Trigger to rising or falling edge

M-Mode

- * 2 channels with 10 ps BIN (INL time interval dependent, see Fig. 4)
- * 70 ps peak-peak (6-8 sigma, sample number dependent)
- * Measurement range 0 ns to > 10 μ s
- * Single hit per Start
- * Minimum pulsewidth 1.5 ns
- * Trigger to rising or falling edge
- * 500 kHz continuous rate per channel

G-Mode

- * 2 channels with 41 ps BIN (INL 1 LSB)
- * Measurement range 0 ns to > 10 μ s
- * 5.5 ns pulse-pair resolution between edges of equal slope with 32-fold multi-hit = 200 MHz peak rate
- * Pulsewidth measurement down to 1.5 ns
- * Trigger to rising and falling edge

Fig. 2: typ. DNL
(differential non-linearity) for R-Mode

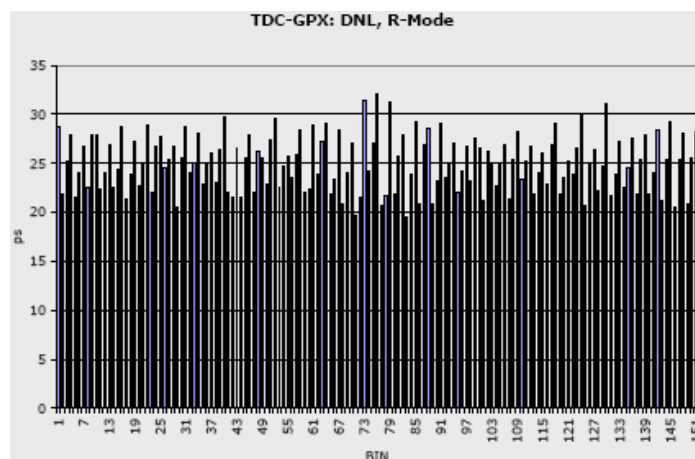
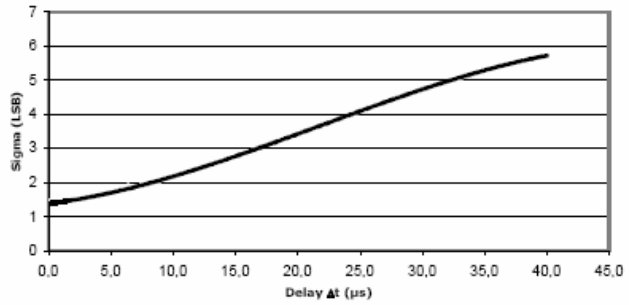


Fig. 3: R-Mode systematic walk of standard deviation
 typ. $1.4 \cdot \text{LSB} + 2.8 \text{ ps} \cdot dt/\mu\text{s}$



M-Mode only:

As a speciality of M-Mode the integral non-linearity shows a deviation of the measured to the real time interval in the near range. The width and height of the non-linear range depends linearly on the MSet value (MSet determines the internal “time-stretch” factor in this mode).

Fig. 4: INL dependent on difference of start-stop time interval.

